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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,627	12/05/2003	Gary L. Swoboda	TI-34654	9072

23494 7590 06/06/2006

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,627	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Swoboda et al., for "Apparatus and method for synchronization of trace streams from multiple processors" filed December 5, 2003, has been examined.

Claims 1-15 are presented for examination.

Claims 1-15 are rejected under 35 USC § 102.

Claim 4 is rejected under 35 USC § 112.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application

No.10729190. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

As per claim 1 of the instant application, claim 1 has the common limitation of

" timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus" with, claim 1 of 10729190. This common limitation performs the same function.

It would have been obvious to one of ordinary skill in the art at the time the invention to use the timing trace, the program counter trace, and the synchronization method of claim 1 of the instant application in the processing unit testing method of claim 1 of 10729190.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because according to the specifications of the instant application using the timing trace, the program counter trace, and the synchronization method is used to test a processing unit. Phillips et al. (U.S. Patent No. 5,321,828) discloses the use of the timing trace (col. 60, lines 56-60), the program counter trace (col. 31, lines 53-56), and the synchronization signals (Fig. 8B) and (Fig. 9, elements 204, 206) in testing of processing units.

Claim Rejections - 35 USC § 112

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "a host processing unit" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Phillips et al. (U.S. Patent No. 5,321,828).

As per claim 1, Phillips discloses during the testing of the operation of a target processing unit (col. 21, lines 54-68), having a plurality of processors (Fig. 1, element 26), a system for synchronizing the trace streams from each of the processors, the system comprising: a plurality of processors, each processor including:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream (col. 60, lines 56-60)

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream (col. 31, lines 53-56)

synchronization apparatus (Fig. 8B) applying sync signals periodically to the timing trace apparatus and to the program counter trace apparatus, the timing trace apparatus including a sync marker in the timing trace stream in response to the sync signal, the program counter trace apparatus including a sync marker in response to the sync signal (Fig. 9, elements 204, 206)

wherein the program counter trace apparatus of each processor is responsive to a global synchronization signal, the program counter trace apparatus of each processor generating global sync marker identifying the occurrence of the global synchronization signal and relating the occurrence of the global synchronization signal to the timing trace stream (Fig. 9, elements 204, 206).

As per claim 2, Phillips discloses the global sync marker includes a global synchronization ID, a program counter address, a timing index and a sync signal ID (col. 31, lines 53-56) and (Fig. 9, elements 204, 206).

As per claim 3, The system as recited in claim 1 further comprising: data trace apparatus responsive to signals from the processing unit (col. 20, lines 30-47), the data

trace apparatus generating a data trace stream, wherein the sync signals are applied to the data trace apparatus, the data trace stream including a sync marker in response to the sync signal (col. 60, lines 56-60) and (col. 31, lines 53-56).

As per claim 4, Phillips discloses a host processing unit can relate the timing trace stream, the program counter trace stream and the data trace stream of all the processors (col. 46, lines 46-48).

As per claim 5, Phillips discloses the method for synchronizing the trace streams of a plurality of processing units (Fig. 1, element 26), the method comprising:

generating a timing trace stream (Fig. 9, element 206)

a program counter trace stream (col. 31, lines 53-56)

and data trace stream for each processing unit (col. 20, lines 30-46)

including sync markers in the in the trace streams of each processing unit permitting synchronization (Fig. 8B) of the trace streams of each processing; and in response to a global synchronization marker applied to each processing unit, including a global synchronization marker in at least one trace stream of each processing unit (col. 20, lines 30-67).

As per claim 6, Phillips discloses in the global synchronization marker, including a global synchronization ID, the global synchronization ID identifying the global synchronization signal resulting in the global synchronization marker (col. 31, lines 53-

56) and (Fig. 9, elements 204, 206).

As per claim 7, Phillips discloses in a processing unit test environment wherein a target processor includes a plurality of processing units (Fig. 1, element 26), each processing unit generating at least one trace stream (col. 20, lines 30-46), a global synchronization marker for inclusion in at least one trace stream for each processor (Fig. 8B), the marker comprising: indicia identifying a global synchronization signal applied to the processing unit issuing the trace stream (Fig. 8B); indicia of the relationship of the occurrence of the global synchronization signal to the clock of the processing unit issuing the trace stream (Fig. 8A); and indicia of the relationship of the occurrence of the global synchronization signal to the processing unit program execution (col. 20, lines 15-27).

As per claim 8, Phillips discloses the indicia of the relationship of the global synchronization signal to the processing unit program execution is a program counter address of the processing unit (col. 31, lines 53-56).

As per claim 9, Phillips discloses a system for testing the operation of a target processing unit (col. 21, lines 54-68), the target processing unit including a plurality of processing units (Fig. 1, element 26), the system comprising:

a global signal synchronization generating unit (Fig. 8A, 8B)

each processing unit including; a central processing unit (Fig. 1, element 26), and trace generating apparatus coupled to the central processing, the trace generating apparatus generating a least one trace stream (Fig. 9, element 206); wherein, the global signal generating unit (Fig. 8A, 8B) applies a global synchronization signal to the trace generating apparatus of each processing unit (Fig. 8B), the global synchronization signal resulting in a global synchronization marker in at least one trace stream (col. 20, lines 30-67).

As per claim 10, Phillips discloses each trace generating unit generates a plurality of trace streams, each processing unit further including a periodic sync signal (Fig. 8B), the periodic sync signal being applied to the trace generating unit, the trace generating unit adding indicia to the plurality trace streams permitting the plurality of trace streams to be synchronized (col. 20, lines 30-67).

As per claim 11, Phillips discloses the global synchronization marker includes a global synchronization identification value and a value related to the processing unit clock (col. 31, lines 53-56) and (Fig. 8A).

As per claim 12, Phillips discloses a host processing unit (col. 46, lines 46-48), the host processing unit using the trace streams to reconstruct the operation of the target processing unit (col. 20, lines 44-46).

As per claim 13, Phillips discloses the global synchronization markers permit the operation of the plurality of processors to be correlated (Fig. 8A, 8B).

As per claim 14, Phillips discloses the method of synchronizing the testing (col. 21, lines 54-68) of a plurality of processing units (Fig. 1, element 26), each processing unit including a trace generating unit for generating a plurality of trace streams, the method comprising: applying a global synchronization signal to the trace generating unit of each processing unit (Fig. 8A, 8B); generating in at least one trace stream of each processing unit a global synchronization marker in response to the global synchronization signal (col. 20, lines 30-67).

As per claim 15, Phillips discloses each trace stream of a processor includes sync markers relating the plurality of trace streams (col. 20, lines 30-47).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Shiell (U.S. Patent No. 6,041,176), "Emulation devices utilizing state machines".

Kashiwagi (U.S. Patent No. 4,780,819), "Emulator system utilizing a program counter and a latch coupled to an emulator memory for reducing fletch line of instructions stored in the emulator memory".

Oguma et al. (U.S. Patent No. 5,132,971), "In-circuit emulator".

Circello et al. (U.S. Patent No. 5,737,516), "Data processing system for performing a debug function and method therefor".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER